

## **Abstract**

A dynamic random access memory (DRAM) features an address counter strobe test mode device including a reference pulse generator, an address counter strobe test mode unit, an internal address counter unit, and an address decoding unit. The reference pulse generator receives an external clock signal and generates an internal clock signal. The address counter strobe test mode unit receives the internal clock signal and outputs an address strobe signal, wherein a pulse width and a pulse generating time of the address strobe signal are regulated in response to a plurality of control signals outputted from a mode register set. The internal address counter unit receives an external address signal and outputs an internal address signal in response to the address strobe signal. The address decoding unit decodes the internal address signal. As a result, the address counter strobe test mode device prevents mis-operations caused by mis-addressing in the DRAM.